**Solutions Calculator Club**

**Project Documentation**

Instruction Register, Control and OUTPUT Logic Module

**Instruction Register Circuit Function:**

**OUTPUT Display Logic Circuit Function:**

This Module contains a total of 3 EEPROMS

Display EEPROM x4 7 Segment Displays Multiplexing.

Two of the EEPROMS are used in the Control logic to reduce the amount of combinational logic. They are coded in 1 of two ways:

1. The Control Logic circuit is coded with the use of an Arduino Uno and two shift registers.
2. The other is the Manual Programer Circuit (Display EEPROM).

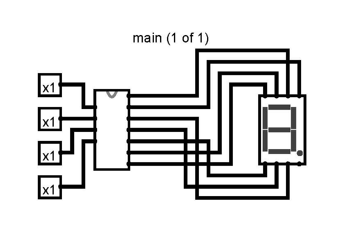
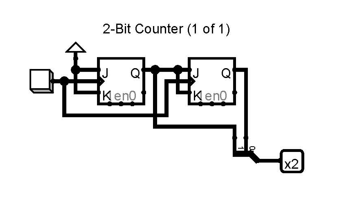


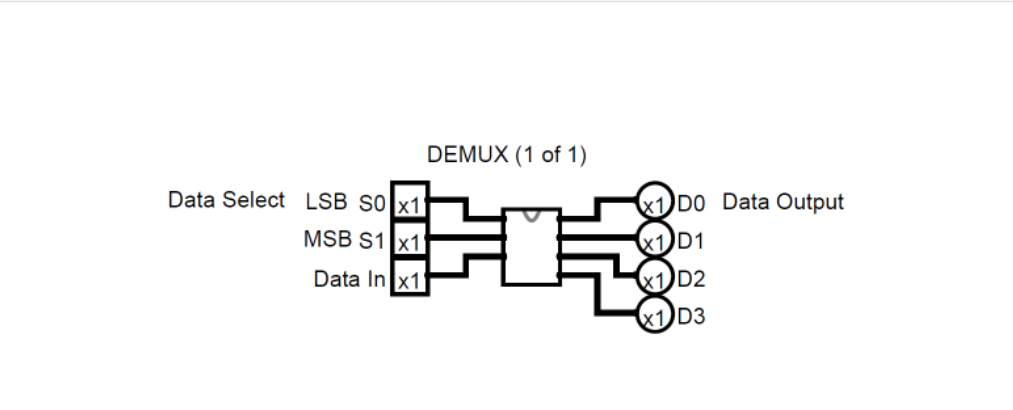
Figure from LOGISIM File.

The figure above of the 7 segment display is used in the OUTPUT Display of the 8-Bit Computer. There are four wired in parallel that use select and multiplexing to display value on the appropriate 7 segment display. The far right display is the 1’s place left from there is the 10’s and 100’s. The leftmost display is the (-) sign when the 2’s complement toggle mode is set.

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**Figure from LOGISIM File**

The INPUT to this couter is from a seperat 555 Clock than the System Clock. The OUTPUT of this counter is the select INPUT of the Multiplexer that lets the EEPROM in this circuit know what diplay is active for what Decimal coded Binary to Display.



**Figure of Multiplexing from LOGISIM File**

**Control Logic Circuit Function:**

The Control Unit is a component in a computer that is responsible for selecting the right registers to pass in as inputs and configuring the ALU to perform the right operation. For an ADD instruction, the Control Unit enables Register B and feeds its value into the first input of the ALU. It also enables Register A and feeds it into the second ALU input. The ALU itself can perform several different operations. The Control Unit must configure it to perform an ADD operation by passing in the ADD opcode. Finally, the output should be saved into Register A.

The CPU is made up of two parts: the control unit and the arithmetic logic unit. The control unit is responsible for fetching instructions from memory and decoding them. The arithmetic logic unit is responsible for executing the instructions.

The Instruction Register (Step)

| Instruction | Address | Binary |
| --- | --- | --- |
| LDA 14 | 0000 | 00011110 |
| ADD 15 | 0001 | 00101111 |
| OUT | 0010 | 11100000 |
|  | 1110 | 00011100 (28) |
|  | 1111 | 00001110 (14) |

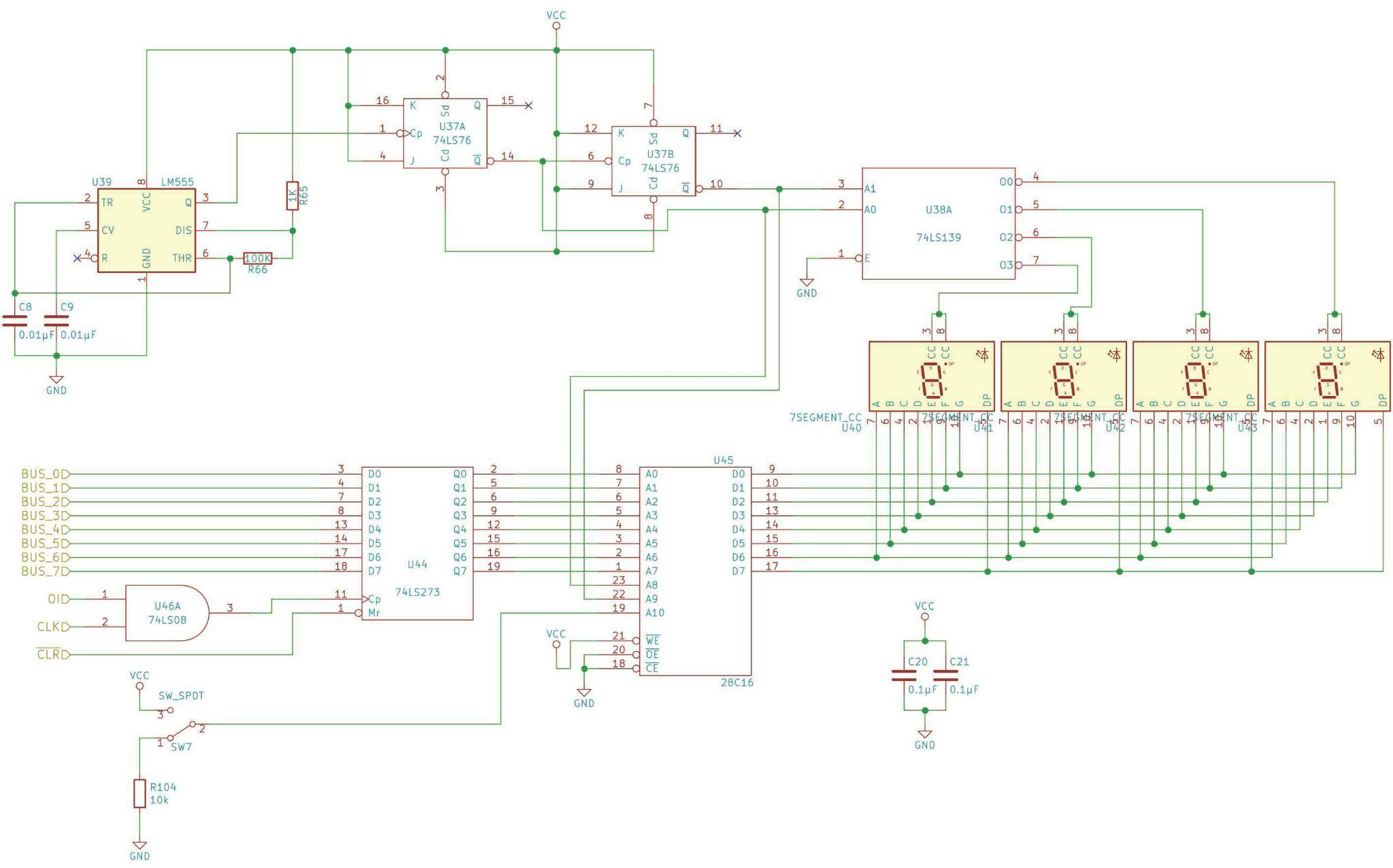
| **LDA 14** | **ADD 15** | **OUT** |
| --- | --- | --- |
| The Fetch Command=  CO MI  RO II  CE | The Fetch Command=  CO MI  RO II  CE | The Fetch Command=  CO MI  RO II  CE |
| IO MI  RO AI | IO MI  RO BI  EO AI | AO OI |

Table above contains micro instructions called control words. The top row is the defined instruction; each instruction has a Fetch Phase, Decode Phase and an Execute Phase.

The Colorful image on the previous page is used to illustrate the function of the CPU. The Addresses of the RAM have already been programmed with OPT Codes and Address 14 and 15 have data values which the ALU will perform the operations on.

If You are wondering, the answer is 42.

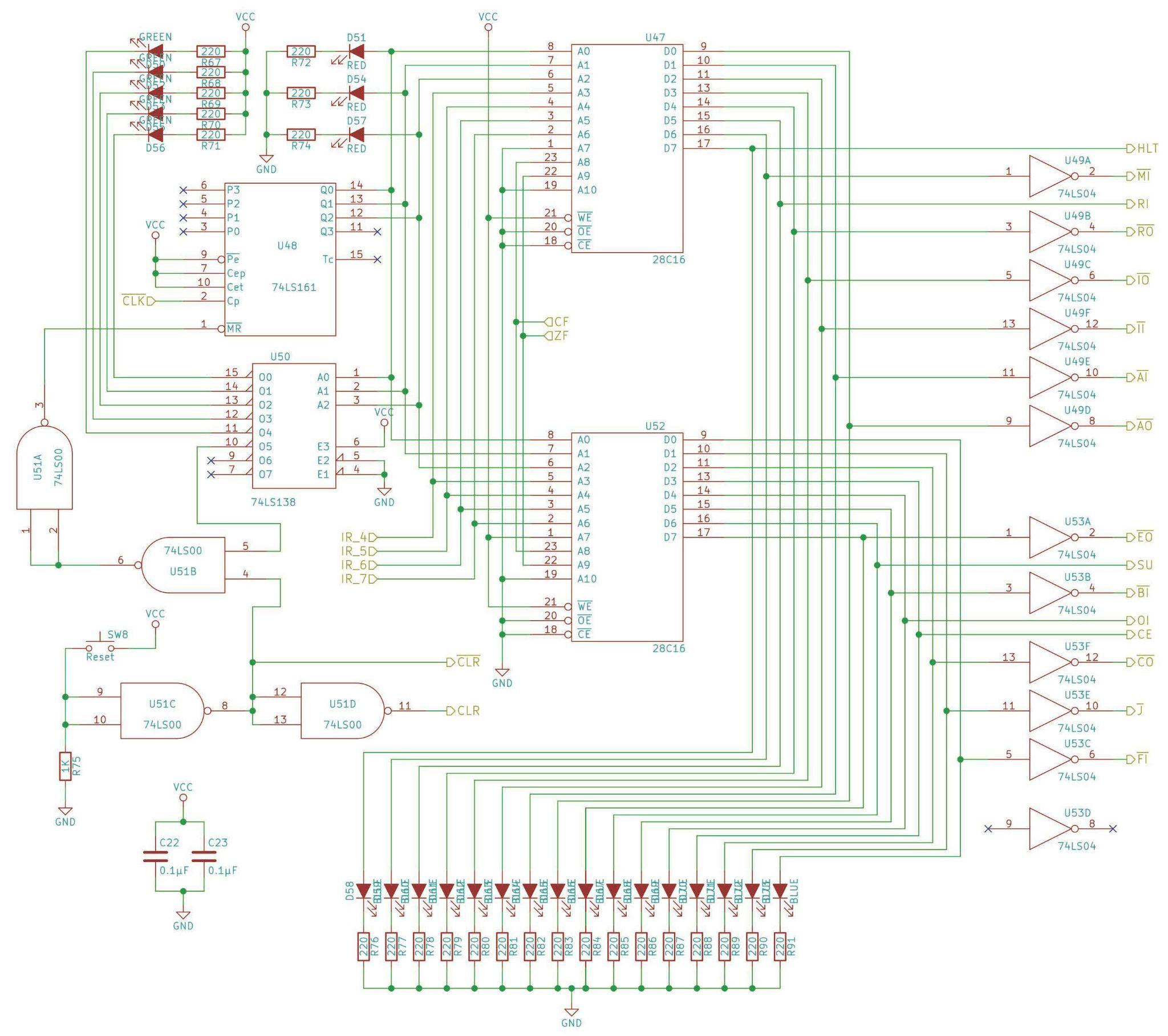
**OUTPUT Display Circuit Schematic:**

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**Parts List** ……………………………………………………………………………

| OutPut Register Module: | | | | | |
| --- | --- | --- | --- | --- | --- |
|  | QN | QIn | **DigiKey Part Number** | **Description** | **Alternate Part** |
|  | 1 |  | 1988-1060-ND | Breadboard |  |
|  | 1 |  | LM555CNNS/NOPB-ND | [555 timer](https://eater.net/datasheets/lm555.pdf) |  |
|  | 1 |  |  | [74LS08 Quad AND gate](https://eater.net/datasheets/74ls08.pdf) |  |
|  |  |  | 296-33952-5-ND  296-2085-5-ND | [74LS107 Dual J/K flip-flop](https://eater.net/datasheets/74ls107.pdf)  [(substitute for 74LS76; check pinout!)](https://eater.net/datasheets/74ls107.pdf) | 74HCT109 |
|  | 1 |  | 296-1640-5-ND | [74LS139 Dual 2-to-4 line decoder/demultiplexer](https://eater.net/datasheets/74ls139.pdf) |  |
|  | 1 |  | 296-33970-5-ND | [74LS273 8-bit D register](https://eater.net/datasheets/74ls273.pdf) |  |
|  | 1 |  |  | [28C16 16K EEPROM](https://eater.net/datasheets/28c16.pdf) |  |
|  | 1 |  |  | SW\_SPDT |  |
|  | 1 |  |  | 10kΩ resistor |  |
|  |  |  |  |  |  |
|  | 2 |  |  | 0.01µF capacitor |  |
|  | 2 |  |  | 0.1µF capacitor |  |

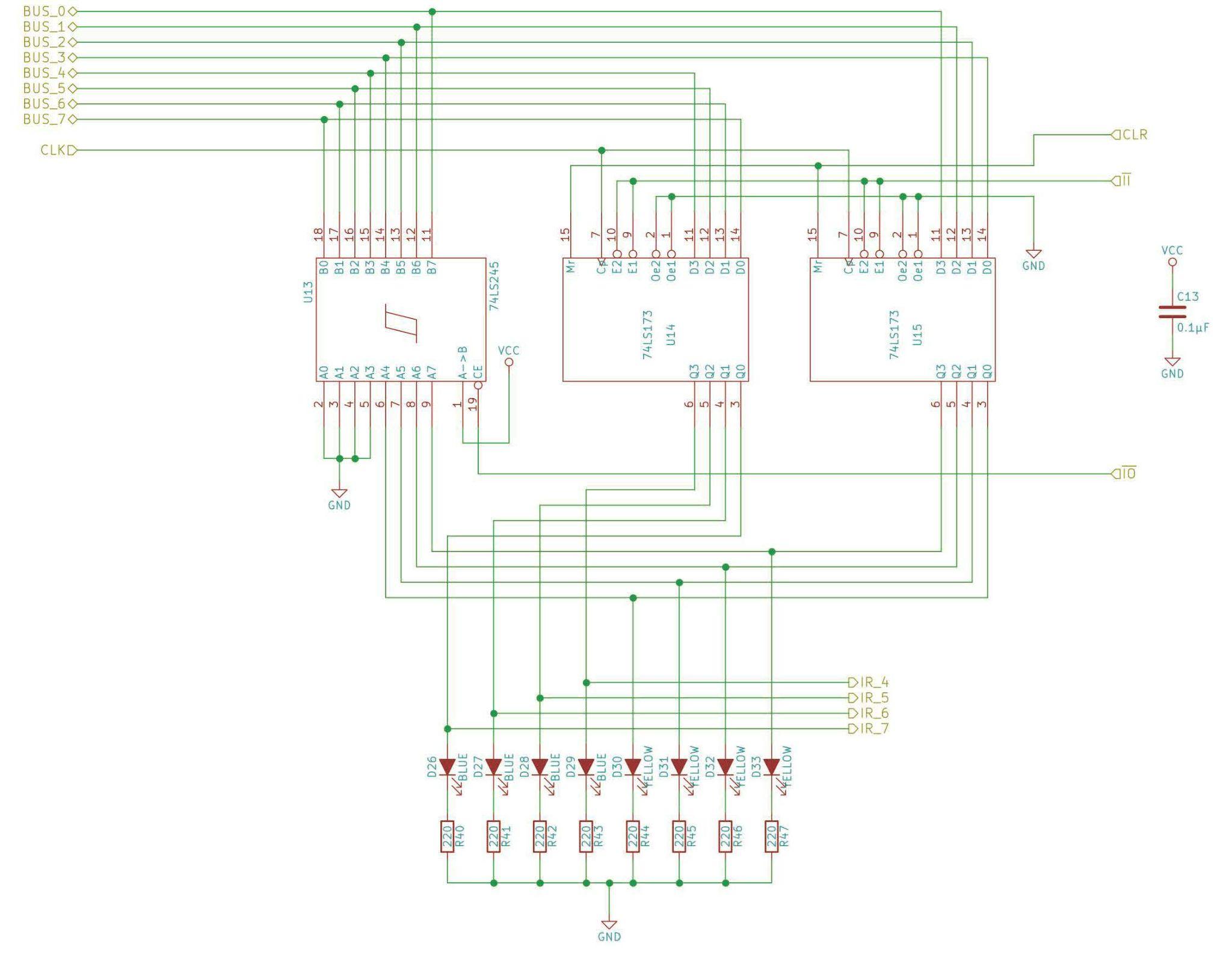
**Control Logic Circuit Schematic:**

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**Control Logic Circuit Parts List:**

| CPU Control Logic Module: | | | | | |
| --- | --- | --- | --- | --- | --- |
|  | QN | QIn | **DigiKey Part Number** | **Description** | **Alternate Part** |
|  | 1 |  | 1988-1060-ND | Breadboard |  |
|  | 1 |  | 296-1626-ND | [74LS00 Quad NAND gate](https://eater.net/datasheets/74ls00.pdf) |  |
|  | 2 |  | 296-1629-5-ND | [74LS04 Hex inverter](https://eater.net/datasheets/74ls04.pdf) |  |
|  | 1 |  | 296-1646-5-ND | [74LS161 4-bit binary counter](https://eater.net/datasheets/74ls161.pdf) |  |
|  | 1 |  | DM74LS138N-ND | [74LS138 3-to-8 line decoder/demultiplexer](https://eater.net/datasheets/74ls138.pdf) |  |
|  | 2 |  |  | [28C16 16K EEPROM](https://eater.net/datasheets/28c16.pdf) |  |
|  | 1 |  |  | 1KΩ resistor |  |
|  | 24 |  |  | 220Ω resistor |  |
|  | 5 | N |  | Green LED |  |
|  | 16 | N |  | Blue LED |  |
|  | 2 |  |  | 0.1µF capacitor |  |

**Instruction Register Circuit Schematic:**

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**Instruction Register Parts List:**

| Instruction Register Module: | | | | | |
| --- | --- | --- | --- | --- | --- |
|  | QN | QIn | **DigiKey Part Number** | **Description** | **Alternate Part** |
|  | 1 |  | 1988-1060-ND | Breadboard |  |
|  | 2 |  | 296-33970-5-ND | [74LS173 4-bit D register](https://eater.net/datasheets/74ls173.pdf) |  |
|  | 1 | 5 | 296-1655-5-ND | 74LS245 (Octal bus transceiver) |  |
|  | 8 |  |  | 220Ω resistor |  |
|  | 4 | N |  | Blue LED |  |
|  | 4 | N |  | Yellow LED |  |
|  | 1 |  |  | 0.1µF capacitor |  |